Calculation of CPI (Cycles Per Instruction)

For the multi-cycle MIPS

Load	5 cycles
Store	4 cycles
R-type	4 cycles
Branch	3 cycles
Jump	3 cycles

If a program has

50%	R-type instructions
10%	load instructions
20%	store instructions
8%	branch instructions
2%	jump instructions

then what is the CPI?

CPI = (4x50 + 5x10 + 4x20 + 3x8 + 3x2)/100 = 3.6

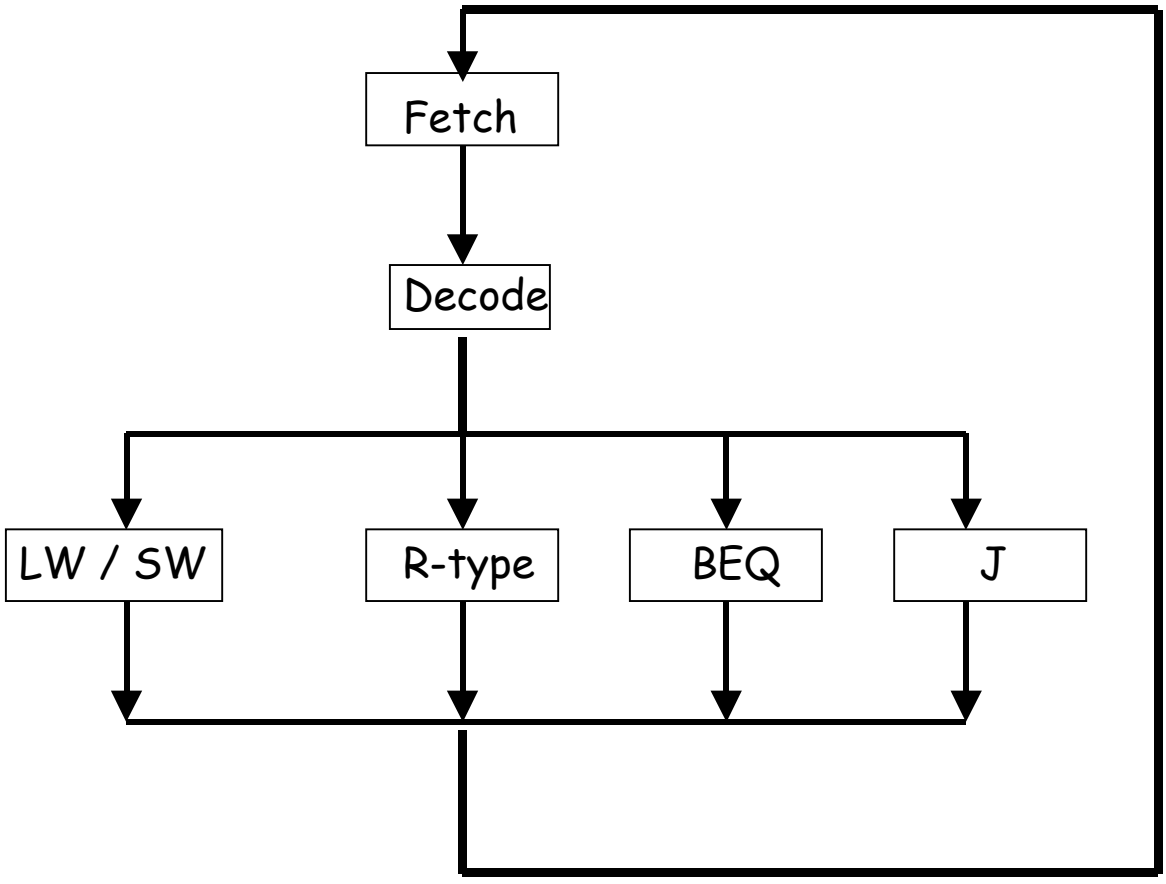
Understanding the Control Unit

The control unit controls the datapath for the proper interpretation of the instructions

Hardware Control (also called Finite State Control)

Micro-programmed Control

Finite State Control



Follow Figures 5.31, 5.37, 5.38 from the textbook. We will discuss them in the class. **Appendix C** contains a detailed design of both the hardware control and the micro-programmed control unit of MIPS

Exceptions

Interrupts, traps, exceptions are similar events. Lead to unplanned detours from the normal control flow.

Occurs very frequently.

Examples of exception

Arithmetic overflow

System Call

Protection violation

Page fault

Misaligned memory access

Undefined instructions

I/O device request

Power failure

Hardware failure

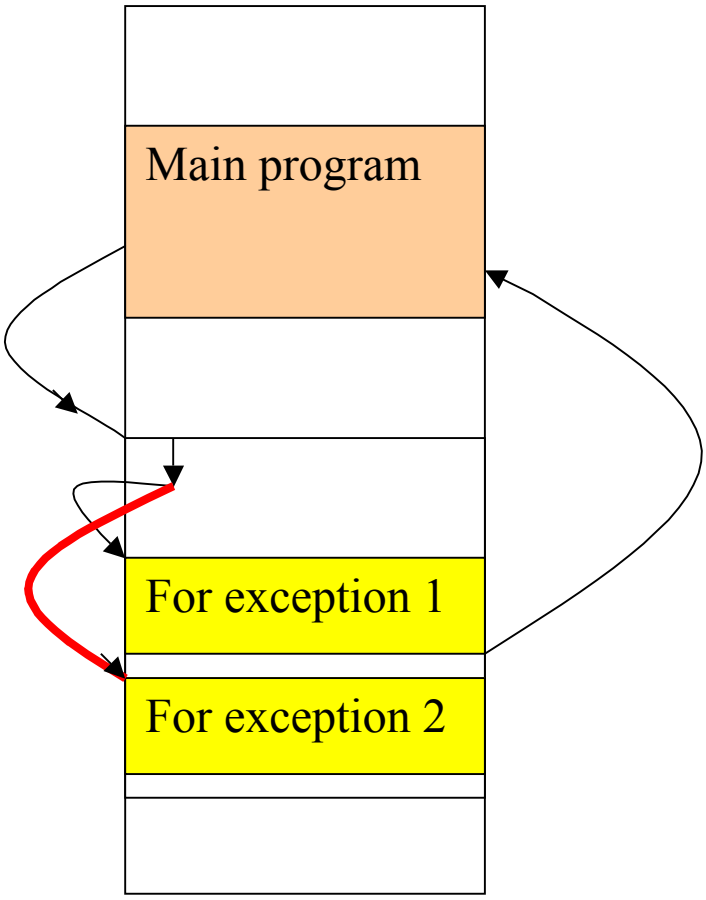
Operator intervention

Exception handling

The control unit checks for exception after the execution of every instruction. Ordinary interrupt forces the PC to a fixed point in the memory, and the code begins with the identification of the cause of the interrupt. In vectored interrupt, control is directly transferred to the starting point of the appropriate handler.

EPC (Exception Program Counter) stores the address of the offending instruction. After the exception is handled (via an exception handling routine), control returns to the EPC.

A Cause register will record the cause of the interrupt. Each bit of a 32-bit cause register will represent a specific type of exception.



The simple version of MIPS handles only two types of exceptions: Study the figures 5:39 and 5.40.