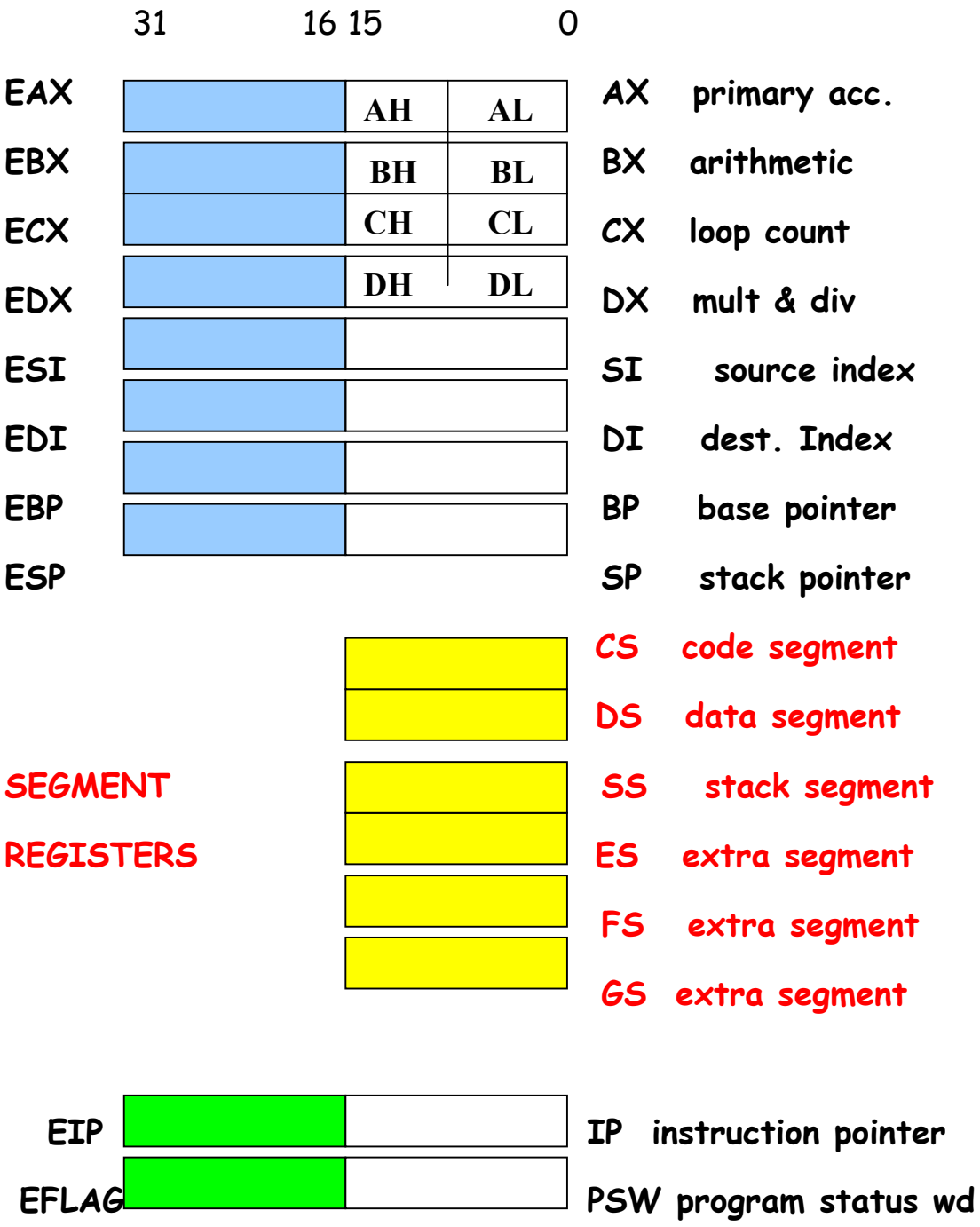
Pentium Family

CISC architecture – executes IA-32 instruction set

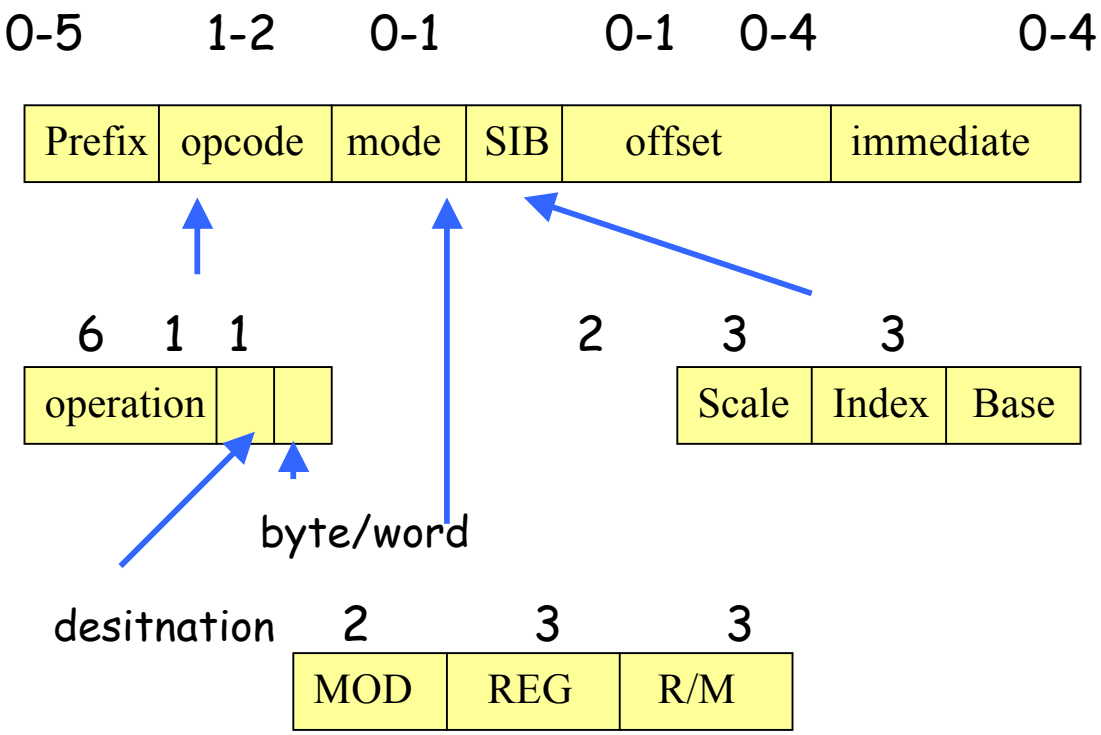
Year	Processor	Clock	L1cache KB	L2 cache KB
1993	Pentium	233-300 MHz		
1995	Pentium Pro	100-200 MHz	8+8	256+1024
1998	Pentium II (MMX added)	233-450 MHz	16+16	256 + 512
1999	Pentium II Xeon	400-450 MHz	16+16	512 + 2048
1999	Celeron	500-900 MHz	16+16	128
1999	Pentium III (70 new MMX instructions)	450-1100 MHz	16+16	256+512
2000	Pentium III		16+16	1024+2048
2001	Xeon	700-900 MHz	8+8	256+512
	Pentium 4 (NetBurst)	1.3 – 2.1 GHz		

All Intel processors are backward compatible.

Intel Pentium Registers



Pentium Instruction Formats



Tells us about the operand

Complex, irregular, and suffers from the legacy of some bad irreversible design decisions made in the past.

Pentium instruction formats

Two operands: One operand is a Register (REG field), and the other specified by MOD and R/M.

R/M	MOD=00	MOD=01	MOD=10	MOD=11
000	M[EAX]	M[EAX+ Offset 8]	M[EAX+ Offset 32]	EAX or AL
001	M[ECX]	M[ECX+ Offset 8]	M[ECX+ Offset 32]	ECX or CL
010	M[EDX]	M[EDX+ Offset 8]	M[EDX+ Offset 32]	EDX or DL
011	M[EBX]	M[EBX+ Offset 8]	M[EBX+ Offset 32]	EBX or BL
100	SIB	SIB with Offset 8	SIB with Offset 32	ESP or AH
101	Direct	M[EBP+ Offset 8]	M[EBP+ Offset 32]	EBP or CH

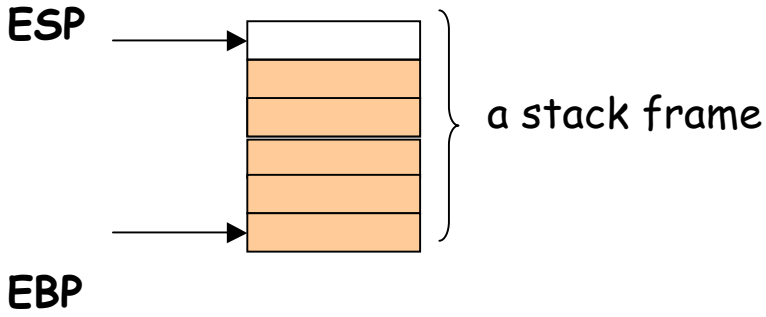
- **Using SIB, operand address = Base register + index register x scale factor (1/2/4) + offset.**
- **Lack of orthogonality is disturbing**

Observations about Pentium Instructions

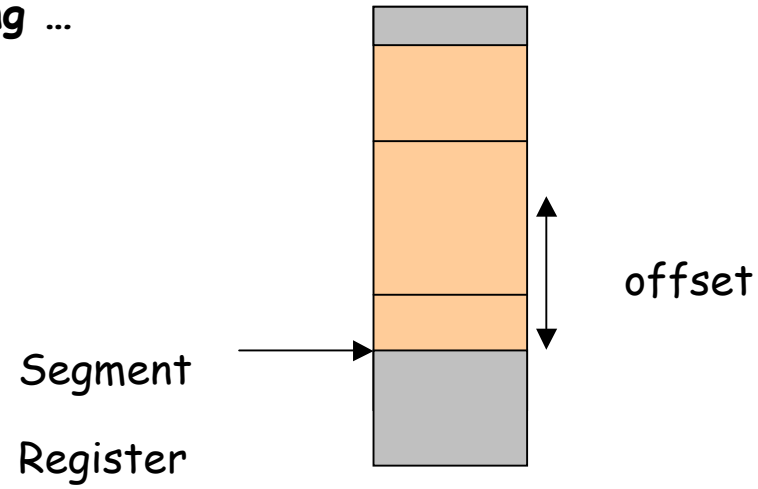
The burden of backward compatibility…

Real mode	Runs 8088 programs.
Virtual 8086 mode	Runs 8086 programs
Protected mode	Works like Pentium

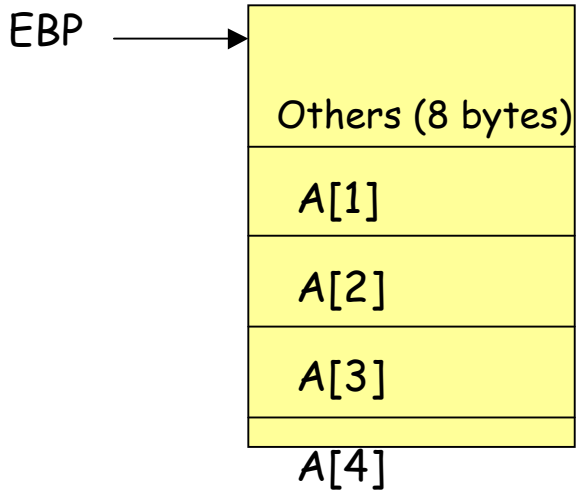
Use of EBP and ESP…



Pentium addressing …



What is SIB?



Useful for addressing the elements of an array

Let each element be 32 bits, i.e 4 bytes.

Store the array index i in EAX.

Address of A[i] = EBP + 4*EAX + 8

What are MMX instructions?

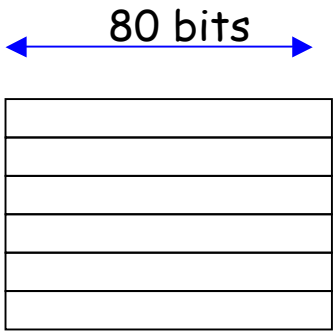
Supports multimedia operations

Can store 8-bit colors for 8 pixels

in one MMX register and execute

SIMD instructions to accelerate

the speed of graphics



FP-cum-MMX

What are Prefix bytes?

Attributes to instructions…

REP ⟨instruction⟩

Repeat the instruction until ECX=0

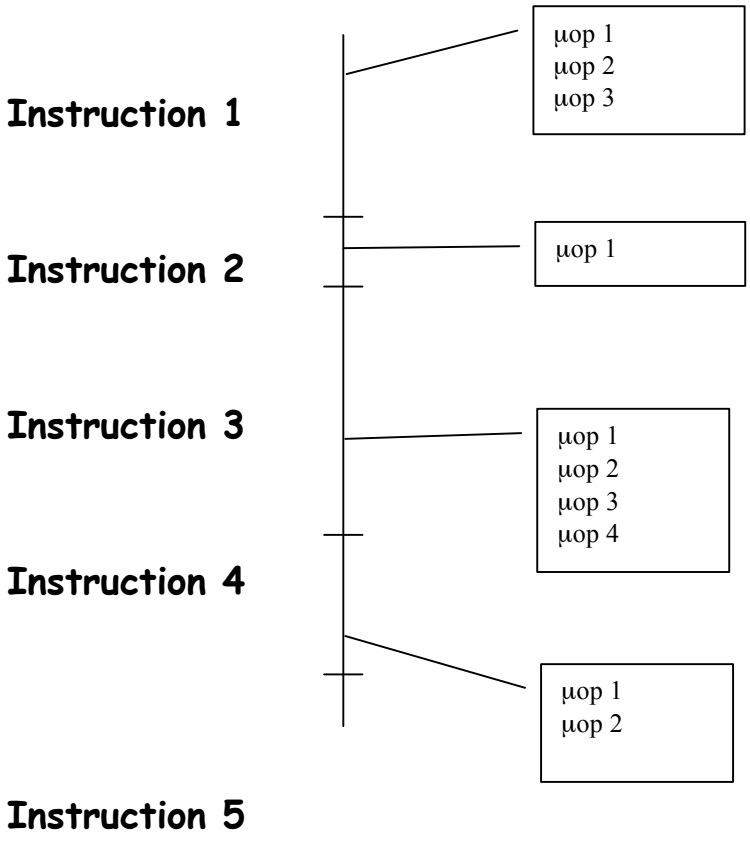
REPZ ⟨instruction⟩

Repeat the instruction until Z-flag is set.

LOCK ⟨instruction⟩

Lock the memory bus until the instruction execution is complete.

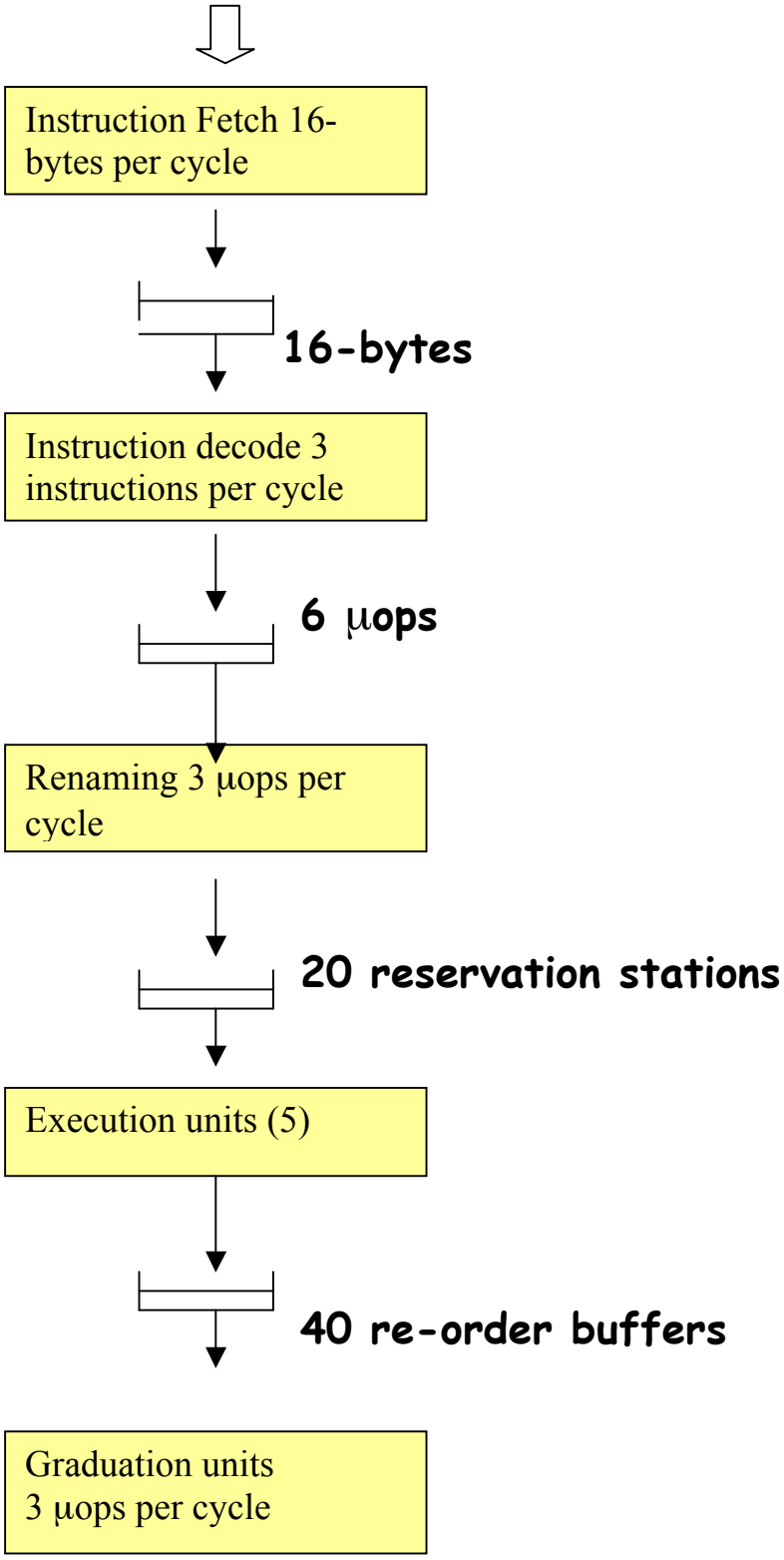
Case Study : Design of Pentium Pro



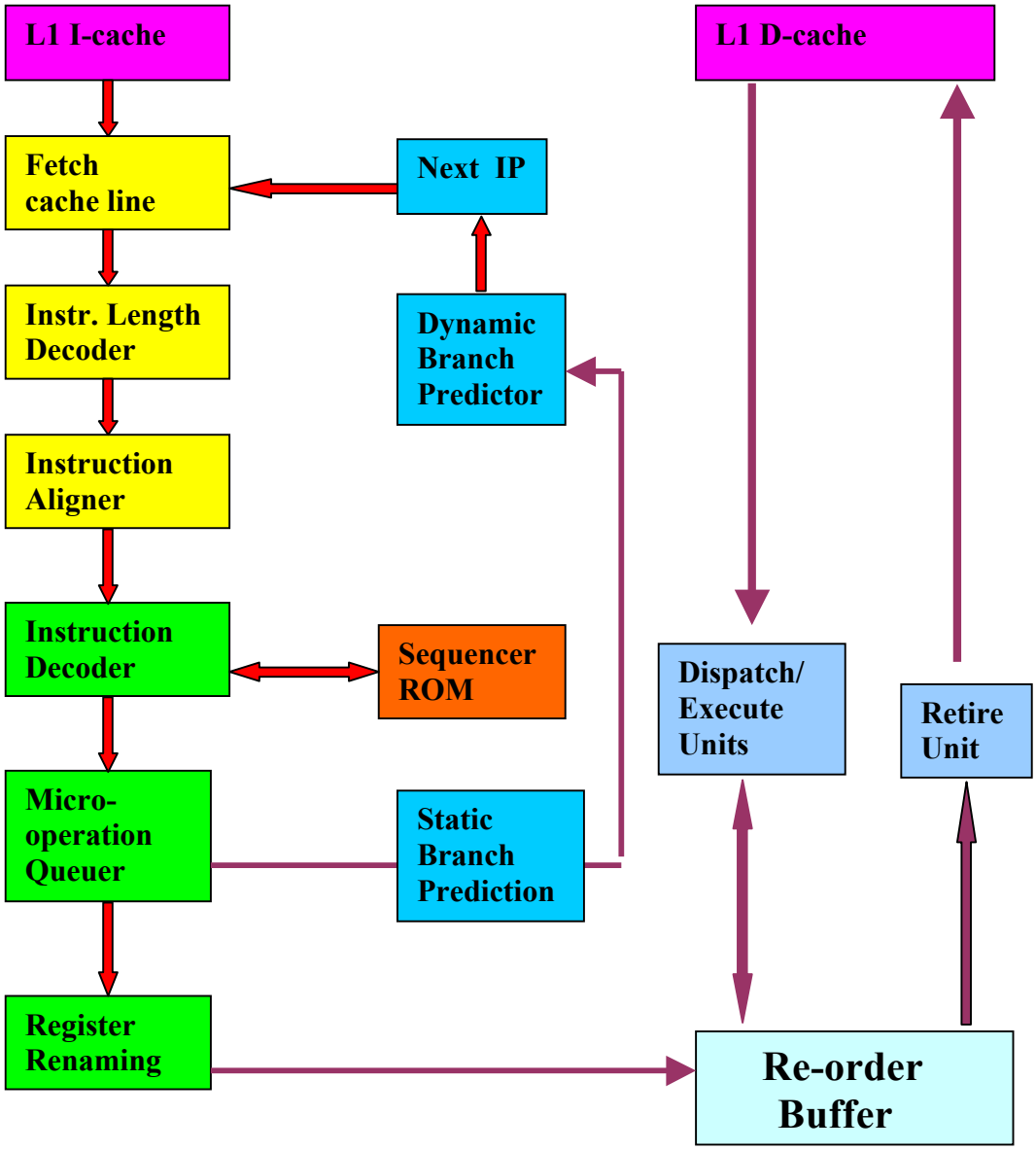
- Each instruction is converted into a sequence of μops that are RISC like instructions. This makes the pipeline much deeper and branch penalty increases.

- Uses a 512-entry 2-level branch predictor

Pentium (P6) Microarchitecture outline



A closer look



Pentium 3 vs Pentium 4

	Pentium 3	Pentium 4
Pipeline depth	10	20
Buffering of results	40	128
Integer units	5	7
Clock	1 GHz	>2 GHz
BTB size	512	4096
L2 cache bandwidth		higher