Designing the MIPS Processor

Chapter 5

We will study the design of a simple version of MIPS that can support the instructions

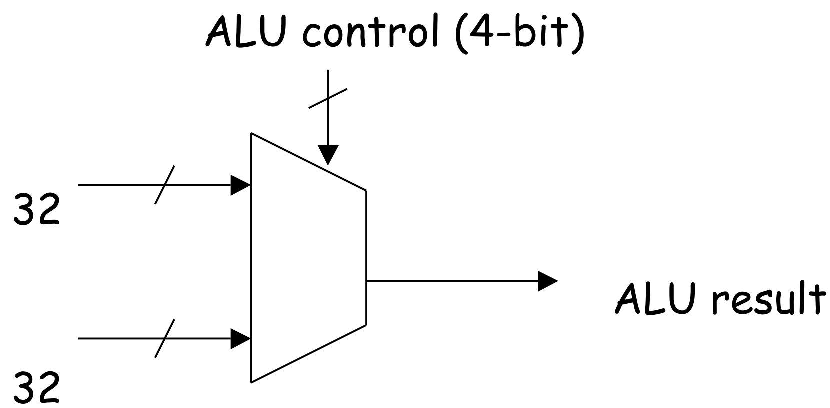
- I-type instructions LW, SW
- R-type instructions, like ADD, SUB
- Conditional branch instruction BEQ
- J-type branch instruction J

Follow the class lectures.

The instruction formats

	6-bit	5-bit	5-bit	5-bit	5-bit	5-bit
LW	op	rs	rt	immediate		
SW	op	rs	rt	immedeiate		
ADD	op	rs	rt	rd	0	func
SUB	op	rs	rt	rd	0	func
BEQ	op	rs	rt	immediate		
J	op		address			

ALU control



ALU control input	ALU function
0000	AND
0001	OR
0010	add
0110	sub
0111	Set less than
etc	etc

How to generate the ALU control input? The control unit first generates a 2-bit ALU op from the opcode of the instruction. This information is combined with the function field of some of the R-type operations to generate the 3-bit control input.

Design of MIPS

Study the datapath, control unit, and the performance of the simple version of MIPS that executes every instruction in one cycle.

Understand the functionality of the building blocks.
Observe the role of the control signals.

Relevant figures: 5.1-5.22