**Multiplexor**

It is a *many-to-one switch*, also called a *selector*.

A 2-to-1 mux

\[ F = \overline{S}. A + S. B \]

**Specifications of the mux**

- \( S = 0, F = A \)
- \( S = 1, F = B \)

Exercise. Design a 4-to-1 mux.
Another design of a multiplexor
Demultiplexors

A demux is a one-to-many switch.


So,  \( X = S \cdot A \), and \( Y = S \cdot B \)

Exercise. Design a 1-4 demux.
A 1-bit ALU

Understand how this circuit works.

Need to add one more input to the mux to implement **slt**
Converting an adder into a subtractor

\[
A - B \quad \text{(here - means arithmetic subtraction)}
\]

\[
= A + 2\text{'s complement of } B
\]

\[
= A + 1\text{'s complement of } B + 1
\]

1-bit adder/subtractor

For subtraction, \( B \text{ invert} = 1 \) and \( \text{Carry in} = 1 \)
1-bit ALU for MIPS

Assume that it has the instructions add, sub, and, or, slt.

Less will be used to detect if the 32-bit number $A$ is less than the 32-bit number $B$.

We now implement $\text{slt}$ (If $A < B$ then Set = 1 else Set = 0)
A 32-bit ALU for MIPS